What is claimed is:

1. A packet transfer apparatus for switching and transferring a cell signal among first and second nodes and a routing device, the nodes having each an interface for the cell signal, the routing device having an interface for the cell signal and determining an outgoing route for the cell signal according to destination data contained in the cell signal, the cell signal being made from a packet signal that contains the destination data, the packet transfer apparatus comprising:

a switch for making a connection path among the nodes and routing device;

a memory for storing outgoing route data for a cell signal; and

a shortcut controller for monitoring outgoing route data contained in a cell signal coming from the routing device, storing the outgoing route data in the memory, checking an input cell signal to see if outgoing route data contained in the input cell signal is equal to the outgoing route data stored in the memory, and if they are equal to each other, controlling the switch to form a shortcut between the first node through which the input cell signal has been received and the second node from which the input cell signal is going to be sent out, and transferring the input cell signal from the first node to the second node through the shortcut.

2. The apparatus of claim 1, wherein the first and second nodes and packet transfer apparatus form an ATM apparatus.

3. The apparatus of claim 2, wherein the cell signal is an AAL5 ATM signal.

4. The apparatus of claim 2, wherein the output route data stored in the memory includes a destination address and an outgoing port number.

5. A packet transfer apparatus for switching and transferring a cell signal among first and second nodes and a routing device, the nodes having each an interface

for the cell signal, the routing device having an interface for the cell signal and determining an outgoing route for the cell signal according to destination data contained in the cell signal, the cell signal being made from a packet signal that contains the destination data, the packet transfer apparatus comprising:

a switch for making a connection path among the nodes and routing device;

a memory for temporarily storing outgoing route data for a cell signal; and

a shortcut controller for monitoring source data contained in a cell signal coming from one of the nodes, storing the source data as outgoing route data in the memory, checking an input cell signal to see if outgoing route data contained in the input cell signal is equal to the outgoing route data stored in the memory, and if they are equal to each other, controlling the switch to form a shortcut between the nodes, and transferring the input cell signal through the shortcut from one of the nodes through which the input cell signal has been received to the other from which the input cell signal is going to be sent out.

6. The apparatus of claim 5, wherein the first and second nodes and packet transfer apparatus form an ATM apparatus.

7. The apparatus of claim 6, wherein the cell signal is an AAL5 ATM signal.

8. The apparatus of claim 6, wherein the output route data stored in the memory includes a source address and an incoming port number.

9. A packet transfer apparatus for switching and transferring a frame signal among first and second nodes and a routing device, the nodes having each an interface for the frame signal, the routing device having an interface for the frame signal and determining an outgoing route for the frame signal according to destination data contained in the frame signal, the frame

signal being made from a packet signal that contains the destination data, the packet transfer apparatus comprising:

a switch for making a connection path among the nodes and routing device;

a memory for storing outgoing route data for a frame signal; and

a shortcut controller for monitoring outgoing route data contained in a frame signal coming from the routing device, storing the outgoing route data in the memory, checking an input frame signal to see if outgoing route data contained in the input frame signal is equal to the outgoing route data stored in the memory, and if they are equal to each other, controlling the switch to form a shortcut between the first node through which the input frame signal has been received and the second node from which the input frame signal is going to be sent out, and transferring the input frame signal from the first node to the second node through the shortcut.

10. The apparatus of claim 9, wherein the first and second nodes and packet transfer apparatus form a frame relay apparatus.

11. The apparatus of claim 10, wherein the output route data stored in the memory includes a destination address and an outgoing port number.

12. A packet transfer apparatus for switching and transferring a frame signal among first and second nodes and a routing device, the nodes having each an interface for the frame signal, the routing device having an interface for the frame signal and determining an outgoing route for the frame signal according to destination data contained in the frame signal, the frame signal being made from a packet signal that contains the destination data, the packet transfer apparatus comprising:

a switch for making a connection path among the nodes and routing device;

a memory for temporarily storing outgoing route data for a frame signal; and

a shortcut controller for monitoring source data contained in a frame signal coming from one of the nodes, storing the source data as outgoing route data in the memory, checking an input frame signal to see if outgoing route data contained in the input frame signal is equal to the outgoing route data stored in the memory, and if they are equal to each other, controlling the switch to form a shortcut between the nodes, and transferring the input frame signal through the shortcut from one of the nodes through which the input frame signal has been received to the other from which the input frame signal is going to be sent out.

13. The apparatus of claim 12, wherein the first and second nodes and packet transfer apparatus form a frame relay apparatus.

14. The apparatus of claim 13, wherein the output route data stored in the memory includes a source address and an incoming port number.